A 2.4-GHz Low Noise Amplifier with Inductive Degeneration

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Abstract-This paper describes the design of a low noise amplifier (LNA) employing a single-stage fully differential inductively degenerated cascode topology to achieve a low noise figure, high gain, high linearity, and good isolation between input and output nodes. An in-band return loss (S_{11}) of -13.2dB is obtained with a center frequency of 2.4GHz, while providing 25.8dB of voltage gain (S_{21}) and a bandwidth of 300MHz. The amplifier consumes 5mW of power with a 1.2V supply, has a noise figure (NF) of 2.43dB, and an input referred third intercept point (IIP3) of -4.5dBm. The amplifier schematic has been realized in Cadence Virtuoso using a 65nm process, and the pre-layout performance has been simulated in SpectreRF. The total area of all components before layout is 0.57mm^2.

INTRODUCTION

The low noise amplifier is a crucial component in the front-end of wireless receivers. The role of the LNA is to provide gain, with sufficient linearity for the low power signals that are received by an antenna, without adding substantial noise [1]. In addition to good noise performance, the design is further constrained by low operating voltages, and low power requirements to be suitable in nanometer CMOS process nodes, and battery powered applications. The inductive source degeneration topology presented here was selected among the common LNA topologies for its superior noise performance, and improved linearity. However, the cost of the source inductor is reduced gain [2].

DESIGN PROCEDURE

The design procedure followed for this LNA is an application of the processes outlined in [1] and [3]. The primary goal of this design was to achieve the target specifications listed in table 1. These target specifications, particularly the power consumption, gain, and noise figure constraints drove many of the design decisions. As defined in [3], the transit frequency, f_T of a MOSFET is the frequency at which the small-signal current gain of the device falls to unity. It can be shown that the transit frequency of a device is approximately given by:

$$\omega_T \approx \frac{g_m}{C_{gs}} \quad (1)$$

Where

$$\omega_T = 2\pi f_T \quad (2)$$

ω_T is the transit frequency expressed in radians per second, g_m is the transconductance of the transistor and C_{gs} is the gate-to-source capacitance. For a known DC operating point of a saturated MOSFET, the transconductance and gate-to-source capacitance values can be calculated by:

$$g_m = \sqrt{2\frac{W}{L}u_n C_{ox} I_D} \quad (3)$$

$$C_{gs} = \frac{2}{3}WLC_{ox} + WC_{ov} \quad (4)$$

W and L are the width and length of the transistor, u_n is the electron mobility for an NFET device, C_{ox} is the oxide capacitance per unit area, C_{ov} is the oxide capacitance per unit width, and I_d is the drain current.

The analysis of the MOSFET transit frequency leads directly to impedance matching capability of the inductively degenerated LNA. Providing a 50Ω termination allows maximum power to be transferred to the LNA from the low power signals received by the antenna. To provide adequate matching to 50Ω, inductor L_s was selected to be approximately 1nH. This value lies in the typical range for the topology (0.5 ~ 1nH) [3], and ultimately determines, along with g_m, the values of C_{gs}, and L_g that will be required for matching. The equation governing the input impedance of the LNA is:

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + w_t L_s \quad (5)$$

	Target Specifications	This Design
Power (mW)	< 5	4.999
IIP3 (dBm)	> -10	-4.586
NF (dB)	< 2.5	2.43
S21 (dB)	> 20	25.81
S11 (db)	< -10	-13.2

TABLE I. SPECIFICATION SUMMARY

At the operating frequency of the circuit, 2.4GHz, the first two terms of the input impedance should be designed to be in resonance. Therefore, the equation for the input impedance becomes:

(6) $$Z_{in} \approx w_t L_s$$

By expanding the ω_T term, one can solve for the required C_{gs} to provide a 50Ω input impedance at the calculated operating point.

(7) $$C_{gs} = \frac{g_m L_s}{z_{in}}$$

Note that C_{gs} is also given by (4). The C_{gs} of the transistors in this process were not large enough at the operating point. It was necessary to place an explicit capacitor between the gate and source nodes. This explicit capacitor effectively lowers the transit frequency of the input device. To ensure that the first two terms of (5) are at resonance at the operating frequency, f_0, the condition for resonance can be arranged to produce a value of the gate inductance, L_g.

(8) $$L_g = \frac{1}{(2\pi f_0)^2 C_{gs}} + L_s$$

Lastly, the loading should also be designed to resonate at the operating frequency. An inductive load was chosen over a resistive load to avoid any DC voltage drop across the load that could limit output

Component	Width (um)	Length (um)	Fingers	Multiplier
M1	4	0.8	20	1
M2	4	0.8	20	1
M3	4	0.8	20	1
M4	4	0.8	20	1
M5	2	0.24	20	4
M6	2	0.24	1	1
M7	4	0.8	1	1

TABLE II. LNA MOSFET PARAMETERS

Component	Width (um)	Length (um)	Value	Quantity
Cin	68.5	68.5	9.5pF	2
Lg	344	337	11.1nH	2
Rb	2	25	9.7kΩ	2
Cgs	17	17	300fF	2
Ls	169	163.5	1.13nH	2
CL	23.19	23.19	1.1pF	2
LL	377	363.5	3.96nH	2

TABLE III. LNA PASSIVE COMPONENT PARAMETERS

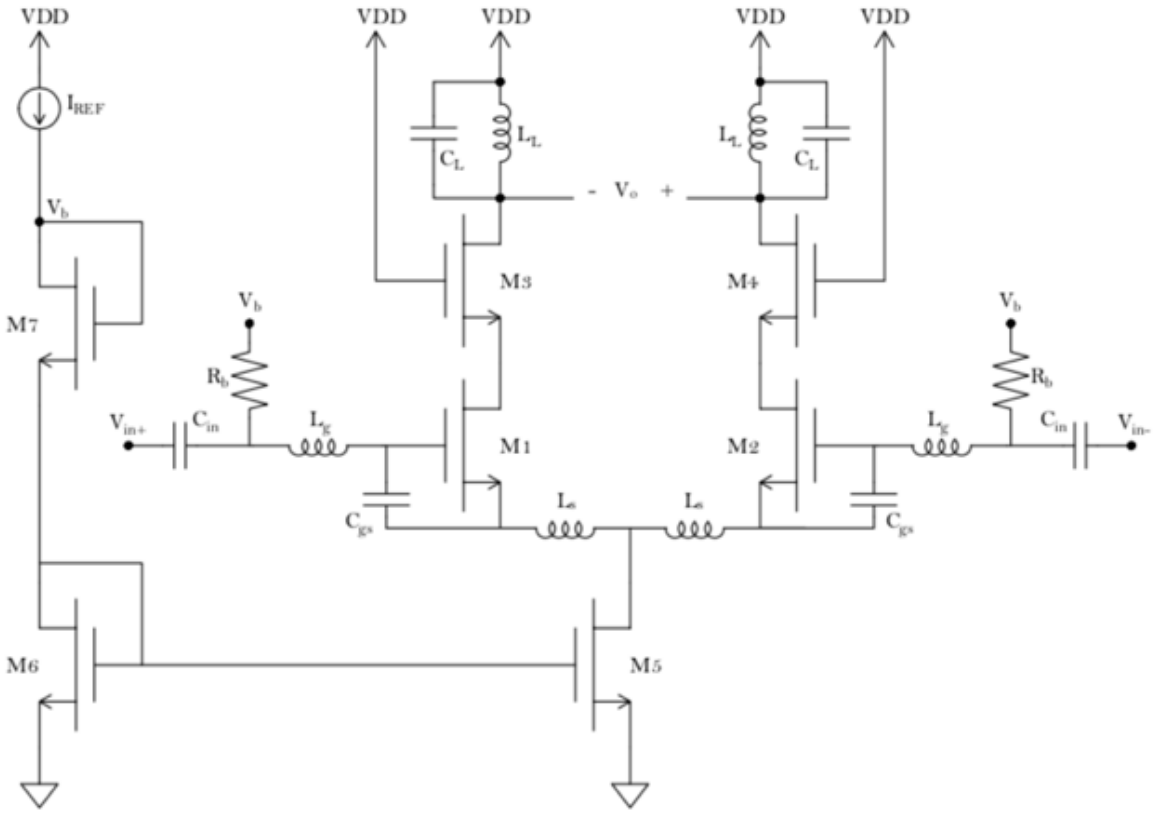


Figure 1. LNA Schematic

voltage swing. While a purely inductive load could resonate with the parasitic capacitance seen at the output node, the low magnitude of this capacitance would have required an inductor that is not feasible to integrate on chip. For this reason, the inductance was chosen to be within the range supported by the process and a capacitor was placed in parallel with the inductance to provide resonance at 2.4GHz. The inductor was also chosen to have a low quality factor for the purpose of providing higher gain to meet the specification. The schematic for the LNA can be seen in figure 1 and sizes are listed in tables 2 and 3.

ITERATION & OPTIMIZATION

Throughout the design process, it was necessary to iterate through the design steps several times to get the specs of the LNA to approach the target specifications. While the preliminary hand calculations and literature provide a great starting point, the simulator allows you to check against your intuition and iterate rapidly. One early observation that is apparent in both the design equations and the simulation results was that using more power quickly improved many of the other specifications. In particular, noise figure has a direct relationship to the transconductance.

$$NF = 1 + g_m R_s \gamma \left(\frac{w_0}{w_T}\right)^2 \quad (9)$$

Where Rs is the source resistance (50Ω) and γ is the drain current thermal noise coefficient. By substituting in (1) and (3) into this equation, one can show that increased transconductance by way of increased drain current can help reduce the NF.

The widths of transistors M1 through M4 were increased to provide more transconductance at a low drain current of 2mA. This drain current was chosen to provide the maximum transconductance while staying within the power specification and was slightly increased later, to meet other specifications as closely as possible. The drain current through each side of the amplifier was set by the tail transistor M5. Together with M6, these two transistors form a current mirror that pulls a multiple of I_{REF} through the circuit. For this design, the reference current was set to 49μA.

As stated above, the choice for L_s drives the other input matching component values. While a wide range of values for C_{gs} were available, that was not the case for L_g. If the value of L_s is decreased further, C_{gs} must also be decreased if the transconductance, and hence, input impedance is to remain the same. This can force the value of the L_g up to a value that is not feasible for this process; either because the inductance is simply too large, or the degraded quality factor adds too much noise to meet the specification. Therefore, these component values were initially selected then later carefully tuned in an iterative process.

The design of the load critically dominates the gain of the amplifier. It was initially challenging to get the voltage gain over 20dB, until realizing that the gain is essentially inversely proportional to the quality factor of the load inductance.

$$A_v = \frac{R_L}{2L_L\omega_0} \quad (10)$$

The equation at first glance seems to imply that one would want a small inductor at the load for high gain, but the R_L / L_L term in this equation can be thought of as the inverse quality factor of the inductor. As the size of the inductor was increased, the inductance was increased, but the quality factor decreased, implying that the parasitic resistance of an inductor increases more rapidly than the inductance as the device dimensions are scaled up. To achieve voltage gain in excess of 20dB, my initial selection for L_L had to be increased, and the parallel capacitance, C_L had to be proportionally decreased to maintain resonance. This step was crucial in getting the desired gain.

CONCLUSIONS

This paper has presented the design of a low noise amplifier in a 65nm CMOS process. The LNA provides a noise figure under 2.5dB with over 25dB of voltage gain in the 300MHz bandwidth. The FOM for this design as specified in (11) is 14.0. All provided target specifications have been met. Possible improvements to this design could be made. The inductors occupy a large area. Methods for decreasing the size of the inductors, or topologies that eliminate them all together could implemented to help conserve area. This design may be able to meet the specifications for an even lower power by scaling the size of the devices with the current, or the implementation of a current reuse topology to achieve high gain for low power cost.

$$FOM = IIP3 - NF - Power(dBm) \quad (11)$$

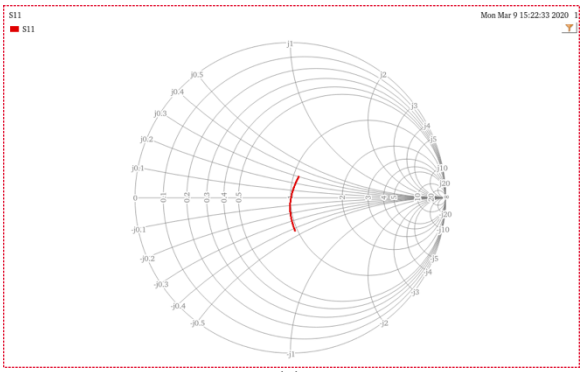
REFERENCES

[1] D.K Shaeffer, T.H. Lee "A 1.5-V 1.5-GHz CMOS low noise amplifier", *IEEE J. Solid-State Circuits*, vol. 32, No. 5, pp. 745-759, May 1997.

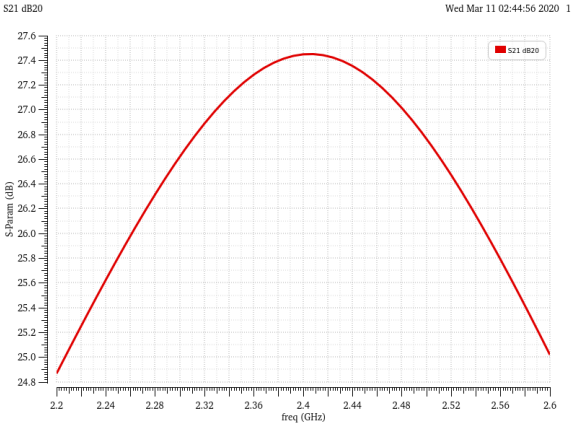
[2] J. Y. Hasani, M. Kamerei, F. Ndagijimana, "Low noise amplifier design in 90nm CMOS technology for near millimetre wave band applications", *IEEE MMWaTT*, Dec. 2009.

[3] B. Razavi, "RF Microelectronics", Prentice Hall. 2012.

APPENDIX



(a)



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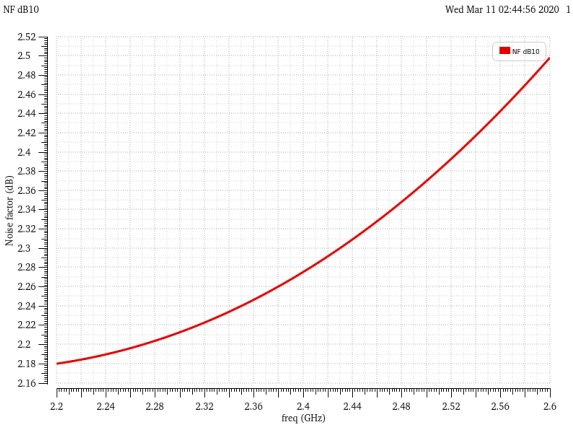

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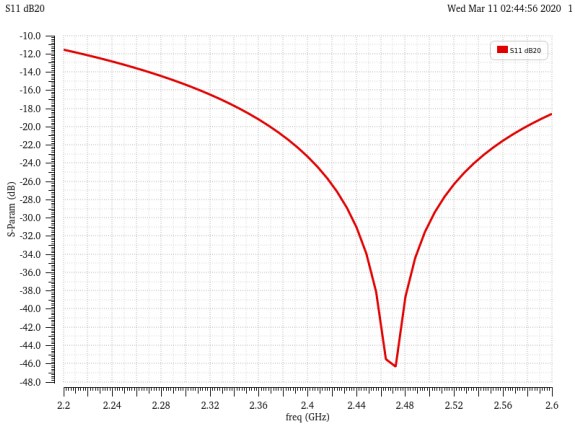
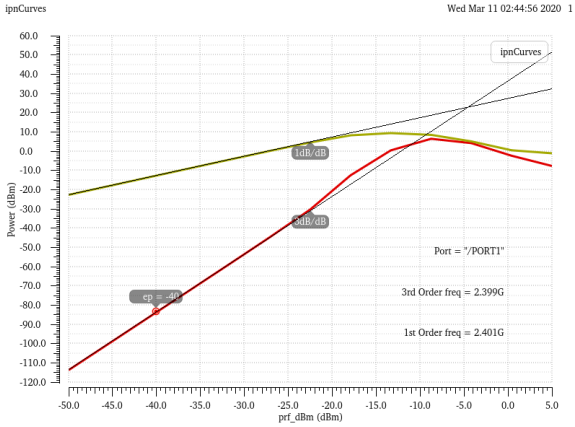


(b)



(d)

Figure 1. Simulation Results: (a) Input Impedance (b) Return loss (S_{11}) (c) Voltage Gain (S_{21}) (d) IIP3 (e) Noise Figure